CLAIMS

What is claimed is:

1. A junction field effect transistor (JFET) comprising:

a heavily doped n^{++} substrate forming a drain region;

an epitaxial n layer comprising a dopant concentration less than that of said n^{++} substrate, said epitaxial n layer formed on top of said n^{++} substrate;

a control structure comprising a p-type gate region implanted into said epitaxial n layer;

a source region sharing a p-n junction with said p-type gate region; and

an altered epitaxial region below said p-type gate region for enlarging a depletion region surrounding said p-type gate region.

2. The JFET as described in Claim 1, wherein said altered epitaxial region comprises a lightly doped n^- layer, wherein said lightly doped n^- layer comprising a second dopant concentration less than that of said epitaxial n layer.

3. The JFET as described in Claim 2, wherein said lightly doped n^- layer is implanted at a higher energy than that associated with said epitaxial n layer.

4. The JFET as described in Claim 1, wherein said altered epitaxial region comprises a lightly doped p^- layer, wherein said lightly doped p^- layer comprising a second dopant concentration less than that of said p-type gate region.

5. The JFET as described in Claim 4, wherein said lightly doped p^- layer is implanted at a higher energy than that associated with said p-type gate region.

6. The JFET as described in Claim 1, further comprising:

a well region formed below a surface of said epitaxial n layer, said oxide well region above said p-type gate region; and

an oxide spacer formed on walls of said well region extending from a surface of said n-type epitaxial layer down into said n-type epitaxial layer, said oxide spacer for directing implantation of dopants into said altered epitaxial region.

7. The JFET as described in Claim 6, wherein said well region is filled with oxide.

8. The JFET as described in Claim 1, wherein said depletion region is further extended into said epitaxial n layer for reducing a junction capacitance between said p-type

gate region and said drain region, without compromising an active region of said JFET.

9. A junction field effect transistor (JFET) comprising:

a heavily doped p^{++} substrate forming a drain region;

an epitaxial p layer comprising a dopant concentration less than that of said p^{++} substrate, said epitaxial p layer formed on top of said p^{++} substrate;

a control structure comprising a n-type gate region implanted into said epitaxial p layer;

a source region sharing a p-n junction with said n-type gate region; and

an altered epitaxial region below said n-type gate region for widening a enlarging region surrounding said n-type gate region.

10. The JFET as described in Claim 9, wherein said altered epitaxial region comprises a lightly doped p^- layer, wherein said lightly doped p^- layer comprising a second dopant concentration less than that of said epitaxial p layer.

11. The JFET as described in Claim 10, wherein said lightly doped p^- layer is implanted at a higher energy than that associated with said epitaxial p layer.

12. The JFET as described in Claim 9, wherein said altered epitaxial region comprises a lightly doped n^- layer, wherein said lightly doped n^- layer comprising a second dopant concentration less than that of said n-type gate region.

13. The JFET as described in Claim 12, wherein said lightly doped n^- layer is implanted at a higher energy than that associated with said n-type gate region.

14. The JFET as described in Claim 9, further comprising:

a well region formed below a surface of said epitaxial p layer, said oxide well region above said n-type gate region; and

an oxide spacer formed on an approximately vertical surface between said well region and said epitaxial p layer, said oxide spacer for directing implantation of dopants into said altered epitaxial region.

15. The JFET as described in Claim 14, wherein said well region is filled with oxide.

16. The JFET as described in Claim 9, wherein said depletion region is further extended into said epitaxial p layer for reducing a junction capacitance between said n-type gate region and said drain region, without compromising an active region of said JFET.

17. A method of fabricating a junction field effect transistor (JFET) comprising:

a) on an n^{++} substrate, forming an n-type epitaxial layer comprising a dopant concentration less than said n^{++} substrate;

b) forming a n^{+} source region disposed on top of a surface of said n-type epitaxial layer, said n^{+} source region having a dopant concentration in between said n^{++} substrate and said n-type epitaxial layer;

c) forming a plurality of well regions in said n-type epitaxial layer surrounding said n^{+} source region;

d) forming a plurality of p-type gate regions surrounding bottoms of said plurality of well regions in said n-type epitaxial layer; and

e) forming an altered n-type epitaxial region below said plurality of well regions for extending depletion regions surrounding said plurality of p-type gate regions into said n-type epitaxial layer without compromising an active region of said JFET.

18. The method of fabricating a JFET as described in Claim 17, further comprising:

before e), forming an oxide spacer on walls of at least one of said plurality of well regions that extend down from said surface into said n-type epitaxial region for directing dopants into said altered n-type epitaxial region in step e).

19. The method of fabricating a JFET as described in Claim 18, further comprising:

filling said well region with oxide.

20. The method of fabricating a JFET as described in Claim 17, wherein e) comprises:

implanting a lightly doped n^- layer directly below said well region, said lightly doped n^- layer comprising a second dopant concentration less than that of said n-type epitaxial layer.

21. The method of fabricating a JFET as described in Claim 17, wherein e) comprises:

implanting a lightly doped p^- layer directly below said well region, said lightly doped p^- layer comprising a second dopant concentration less than that of said p-type gate region.

22. A method of fabricating a junction field effect transistor (JFET) comprising:

a) on an p^{++} substrate, forming an p-type epitaxial layer comprising a dopant concentration less than said p^{++} substrate;

b) forming a p^+ source region disposed on top of a surface of said p-type epitaxial layer, said p^+ source region

comprising a dopant concentration in between said p^{++} substrate and said p-type epitaxial layer;

c) forming a plurality of well regions in said p-type epitaxial layer surrounding said p^{+} source region;

d) forming a plurality of n-type gate regions surrounding bottoms of said plurality of well regions in said p-type epitaxial layer; and

e) forming an altered p-type epitaxial region below said plurality of well regions for extending depletion regions surrounding said plurality of n-type gate regions into said p-type epitaxial layer without compromising an active region of said JFET.

23. The method of fabricating a JFET as described in Claim 22, further comprising:

filling said well region with oxide.

24. The method of fabricating a JFET as described in Claim 22, further comprising:

before e), forming an oxide spacer on walls of at least one of said plurality of well regions, said walls extending down from said surface into said p-type epitaxial region for directing dopants into said altered p-type epitaxial region in step e).

25. The method of fabricating a JFET as described in Claim 22, wherein e) comprises:

implanting a lightly doped p^- layer directly below said well region, said lightly doped p^- layer comprising a second dopant concentration less than that of said p-type epitaxial layer.

26. The method of fabricating a JFET as described in Claim 22, wherein e) comprises:

implanting a lightly doped n^- layer directly below said well region, said lightly doped n^- layer comprising a second dopant concentration less than that of said n-type gate region.